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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: : EXAMINER

JAMAL RAMDANI

SERIAL NO.: NEW DIVISIONAL APPL. :

FILED: HEREWITH : GROUP ART UNIT

FOR: SEMICONDUCTOR STRUCTURE, SEMICONDUCTOR DEVICE, COMMUNICATING DEVICE, INTEGRATED CIRCUIT, AND PROCESS FOR FABRICATING THE SAME

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits, please enter the following Amendment.

IN THE CLAIMS

Please cancel Claims 1-143.

Please add new Claims 144-237.

--144. A semiconductor structure comprising:

a plurality of material layers including:

a monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying at least a portion of the monocrystalline silicon substrate;

an amorphous oxide material located between the monocrystalline perovskite oxide material and the monocrystalline silicon substrate;

a monocrystalline compound semiconductor material overlying at least a portion of the monocrystalline perovskite oxide material; and

a component formed at least partially within one of the plurality of layers.

145. A semiconductor structure as described in claim 144, further comprising a plurality of components formed on or within the monocrystalline compound semiconductor material, the plurality of components forming a first circuit.

146. A semiconductor structure as described in claim 145, wherein a portion of the monocrystalline silicon substrate is exposed, and further comprising a plurality of components forming a second circuit formed on or within the monocrystalline silicon substrate.

147. A semiconductor structure as described in claim 146, wherein the first and second circuits are operatively coupled to form an integrated circuit.

148. A semiconductor structure as described in claim 144, wherein the component is formed on the monocrystalline silicon substrate forming a first component.

149. A semiconductor structure as described in claim 148, wherein a second component is formed on the monocrystalline compound semiconductor material.

150. A semiconductor structure as described in claim 149, wherein the first and second components are operatively coupled to form an integrated circuit.

151. A semiconductor structure as described in claim 144, wherein the monocrystalline compound semiconductor material comprises Group III-V material upon which the component is formed.

152. A semiconductor structure as described in claim 144, wherein the monocrystalline compound semiconductor material comprises Group III-V material with which a first set of components is formed, and wherein a second set of components is formed with the monocrystalline silicon substrate.

153. A semiconductor structure as described in claim 152, wherein the first and second sets of components are operatively coupled to form an integrated circuit.

154. A semiconductor structure as described in claim 153, wherein the first set of components is used in an analog circuit and the second set of components is used in a digital circuit.

155. A semiconductor structure as described in claim 153, wherein the first set of components is used in a digital circuit and the second set of components is used in an analog circuit.

156. A semiconductor structure as described in claim 153, wherein the first set of components is used in an analog circuit and the second set of components is used in an analog circuit.

157. A semiconductor structure as described in claim 153, wherein the first set of components is used in a digital circuit and the second set of components is used in a digital circuit.

158. A semiconductor structure comprising:
a plurality of material layers including:
a monocrystalline silicon substrate;
a monocrystalline perovskite oxide material overlying at least a portion of the monocrystalline silicon substrate;
an amorphous oxide material located between the monocrystalline perovskite oxide material and the monocrystalline silicon substrate;
a monocrystalline compound semiconductor material overlying at least a portion of the monocrystalline perovskite oxide material; and
an electrical component formed at least partially within the monocrystalline compound semiconductor layer.

159. The semiconductor structure of claim 158, wherein the electrical component comprises an active device.

160. The semiconductor structure of claim 158, wherein the electrical component comprises a passive device.

161. The semiconductor structure of claim 158, wherein the electrical component comprises a transistor.

162. The semiconductor structure of claim 161, wherein the transistor comprises a field effect transistor (FET).

163. The semiconductor structure of claim 158, wherein the electrical component comprises a component in an amplifier circuit.

164. The semiconductor structure of claim 163, wherein the amplifier circuit is selected from a group consisting of: a radio frequency amplifier, a power amplifier, a receiving amplifier, and a transmitting amplifier.

165. The semiconductor structure of claim 158, wherein the electrical component comprises a component in an analog circuit.

166. The semiconductor structure of claim 158, wherein the electrical component comprises a component in a digital circuit.

167. A process for fabricating a semiconductor structure that includes a plurality of material layers, comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline substrate;

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a portion of an electrical component in at least one of the plurality of material layers.

168. The process of claim 167, wherein the monocrystalline perovskite oxide film has a thickness less than a thickness that would result in strain-induced defects.

169. The process of claim 167, wherein the electrical component comprises an active device.

170. The process of claim 167, wherein the electrical component comprises a passive device.

171. The process of claim 167, wherein the electrical component comprises a transistor.

172. The process of claim 171, wherein the transistor comprises a field effect transistor (FET).

173. The process of claim 167, wherein the electrical component comprises a component in a digital circuit.

174. The process of claim 167, wherein the electrical component comprises a component in a digital signal processing circuit.

175. The process of claim 167, wherein the electrical component comprises a component in a communication device.

176. The process of claim 167, wherein the electrical component comprises a component in an amplifier circuit.

177. The process of claim 176, wherein the amplifier circuit is selected from the group consisting of: radio frequency amplifier, power amplifier, receiving amplifier, and transmitting amplifier.

178. A semiconductor device comprising:

a monocrystalline silicon layer comprising a first region and a second region;

a first semiconductor component positioned at least partially within the first region;

a monocrystalline oxide layer overlying the second region;

an amorphous oxide layer located between the monocrystalline oxide layer and the monocrystalline silicon layer;

a monocrystalline compound semiconductor layer overlying the monocrystalline oxide layer; and

a second semiconductor component positioned at least partially within the monocrystalline compound semiconductor layer.

179. The semiconductor device of claim 178 wherein the monocrystalline oxide layer is a perovskite.

180. The semiconductor device of claim 178 further comprising an electrical interconnection between the first semiconductor component and the second semiconductor component.

181. The semiconductor device of claim 178 wherein the monocrystalline oxide layer comprises a material selected from the group consisting of: alkaline earth metal titanates, alkaline earth metal zirconates, and alkaline earth metal hafnates.

182. The semiconductor device of claim 181 further comprising an electrical interconnection between the first semiconductor component and the second semiconductor component.

183. The semiconductor device of claim 178 wherein the first semiconductor component comprises a transistor.

184. The semiconductor device of claim 183 wherein the second semiconductor comprises a transistor.

185. The semiconductor device of claim 178 wherein the first semiconductor component is used in a digital circuit and the second semiconductor component is used in an analog circuit.

186. The semiconductor device of claim 185 wherein the first and second semiconductor components are operatively coupled.

187. The semiconductor device of claim 178 wherein the first semiconductor component is used in an analog circuit and the second semiconductor component is used in a digital circuit.

188. The semiconductor device of claim 187 wherein the first and second semiconductor components are operatively coupled.

189. The semiconductor device of claim 178 wherein the first semiconductor component is used in an analog circuit and the second semiconductor component is used in an analog circuit.

190. The semiconductor device of claim 189 wherein the first and second semiconductor components are operatively coupled.

191. The semiconductor device of claim 178 wherein the first semiconductor component is used in a digital circuit and the second semiconductor component is used in a digital circuit.

192. The semiconductor device of claim 191 wherein the first and second semiconductor components are operatively coupled.

193. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate comprising a first region and a second region, the second region having an oxidized surface;

forming a CMOS circuit in the first region;

depositing a material comprising strontium onto the second region having an oxidized surface and reacting the material with the oxidized surface to form a first template layer;

depositing a monocrystalline oxide layer comprising strontium, titanium and oxygen overlying the first template layer by introducing strontium, titanium, and a partial pressure of oxygen to the template layer;

increasing the partial pressure of oxygen to form an amorphous layer of silicon oxide on the second region;

depositing a second template layer overlying the monocrystalline oxide layer;

depositing a layer of a monocrystalline compound semiconductor material comprising gallium and arsenic overlying the second template layer;

forming a semiconductor component at least partially overlying the monocrystalline compound semiconductor material; and

depositing a metallic conductor configured to electrically couple the CMOS circuit and the semiconductor component.

194. The process of claim 193, wherein the CMOS circuit forms digital circuitry and wherein the semiconductor component forms a portion of an analog circuit.

195. The process of claim 193, wherein the CMOS circuit forms digital circuitry and wherein the semiconductor component forms a portion of a digital circuit.

196. A communicating device including an integrated circuit, wherein the integrated circuit comprises:

a monocrystalline silicon substrate;

an accommodating buffer layer overlying at least a portion of the monocrystalline silicon substrate;

an amorphous oxide material located between the accommodating buffer layer and the monocrystalline silicon substrate;

a compound semiconductor portion overlying at least a portion of the accommodating buffer layer, wherein the compound semiconductor portion includes a feature selected from a group consisting of an amplifier, a modulating circuit, and a demodulating circuit; and

the monocrystalline silicon substrate including a digital logic portion coupled to the feature.

197. The communicating device of claim 196 wherein the accommodating buffer layer comprises monocrystalline oxide.

198. The communicating device of claim 197, wherein the compound semiconductor portion has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the accommodating buffer layer.

199. The communicating device of claim 198, wherein the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to the monocrystalline silicon substrate.

200. The communicating device of claim 199, wherein the accommodating buffer layer and the compound semiconductor portion have an effective lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

201. The communicating device of claim 197, wherein:

the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline silicon substrate; and

the accommodating buffer layer and the compound semiconductor portion have an effective lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

202. The communicating device of claim 197, wherein the accommodating buffer layer and the compound semiconductor portion have an effective lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

203. A communicating device including:

a signal transceiving means;

an integrated circuit including:

a monocrystalline silicon substrate including a digital signal processing means;

a monocrystalline perovskite oxide material overlying at least a portion of the monocrystalline silicon substrate;

an amorphous oxide material located between the monocrystalline perovskite oxide material and the monocrystalline silicon substrate;

a compound semiconductor layer overlying at least a portion of the monocrystalline perovskite oxide material, the compound semiconductor layer having an amplifier coupled to the signal transceiving means and the digital signal processing means; and

a unit consisting of one or more of: an input unit and an output unit.

204. The communicating device of claim 203, wherein the communicating device is a portable telephone.

205. The communicating device of claim 203, wherein the communicating device is a cellular telephone.

206. The communicating device of claim 203, wherein the monocrystalline silicon substrate includes a converter selected from a group consisting of: a digital-to-analog converter and an analog-to-digital converter, wherein the converter is coupled to the unit.

207. The communicating device of claim 203, wherein the unit is selected from a group consisting of a keyboard, a microphone, a speaker, a visual display, and a memory means.

208. The communicating device of claim 203, wherein:

the monocrystalline silicon substrate includes a bipolar portion and a field-effect portion; and

the bipolar portion includes a signal modulating means coupled to the digital signal processing means and the amplifier.

209. The communicating device of claim 203, wherein the compound semiconductor layer further includes a signal modulating means.

210. The communicating device of 203, wherein:

the signal transceiving means includes an antenna;

the amplifier is a power amplifier;

the integrated circuit includes a bipolar portion having a radio frequency to intermediate frequency mixer coupled to the power amplifier and the digital signal processing means;

the unit includes a microphone; and

the communicating device further includes a speaker.

211. An integrated circuit comprising:

a monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying at least a portion of the monocrystalline silicon substrate;

an amorphous oxide material located between the monocrystalline perovskite oxide material and the monocrystalline silicon substrate;

a monocrystalline compound semiconductor layer overlying at least a portion of the monocrystalline perovskite oxide material; and

a plurality of active devices located at least partially within or over the monocrystalline compound semiconductor layer.

212. The integrated circuit of claim 211, wherein the integrated circuit further includes passive devices located at least partially within or over the monocrystalline compound semiconductor layer.

213. The integrated circuit of claim 211, wherein the compound semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline perovskite oxide.

214. The integrated circuit of claim 211, wherein the monocrystalline silicon substrate is at least approximately 300 millimeters wide.

215. The integrated circuit of claim 211, wherein the monocrystalline perovskite oxide has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline silicon substrate.

216. The integrated circuit of claim 211, wherein the integrated circuit has at least one feature selected from a group consisting of:

the monocrystalline perovskite oxide layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline silicon substrate; and

the monocrystalline perovskite oxide layer and the monocrystalline silicon substrate have an effective lattice mismatch no greater than approximately 2.0% and a thickness of the monocrystalline perovskite oxide is at least approximately 20 nm.

217. The integrated circuit of claim 211, wherein the monocrystalline perovskite oxide layer and the monocrystalline compound semiconductor layer have an effective lattice mismatch no greater than approximately 2.0% and a thickness of the monocrystalline compound semiconductor layer is at least approximately 20 nm.

218. An integrated circuit comprising:

a monocrystalline silicon substrate having first and second regions;

a monocrystalline compound semiconductor layer overlying the second region of the monocrystalline silicon substrate, the monocrystalline compound semiconductor layer being substantially lattice matched to the monocrystalline

silicon substrate through at least one crystallographically oriented, strain relieved, lattice compensated layer;

an amorphous oxide material located between the monocrystalline compound semiconductor layer and the monocrystalline silicon substrate; and the integrated circuit including:

a first set electrical components formed at least partially in the first region of the monocrystalline silicon substrate and providing digital signal processing; and

a second set electrical components formed at least partially in the monocrystalline compound semiconductor layer and providing analog signal processing.

219. The integrated circuit of claim 218, wherein the first set of electrical components and the second set of electrical components are operatively coupled to each other.

220. The integrated circuit of claim 219, wherein the first set of electrical components and the second set of electrical components are coupled through wire interconnects.

221. The integrated circuit of claim 219, wherein the first set of electrical components and the second set of electrical components are coupled through optical coupling.

222. The integrated circuit of claim 219, wherein the first set of electrical components and the second set of electrical components are coupled together through a combination of electrical and optical coupling.

223. An integrated circuit comprising:

a monocrystalline silicon substrate;

a monocrystalline perovskite oxide layer overlying at least a portion of the monocrystalline silicon substrate;

an amorphous oxide material located between the monocrystalline perovskite oxide layer and the monocrystalline silicon substrate;

a compound semiconductor portion including an optical component overlying the monocrystalline silicon semiconductor substrate; and
a silicon semiconductor portion including an electrical component coupled to the optical component.

224. The integrated circuit of claim 223, wherein the electrical component is a transistor.

225. The integrated circuit of claim 224, wherein the optical component is a laser.

226. The integrated circuit of claim 225, further comprising an optical interconnect between the transistor and the laser.

227. The integrated circuit of claim 226, wherein the optical interconnect comprises a waveguide.

228. The integrated circuit of claim 227, wherein the transistor comprises a CMOS transistor.

229. The integrated circuit of claim 227, wherein the waveguide comprises at least a portion of the monocrystalline perovskite oxide layer.

230. The integrated circuit of claim 223, wherein the compound semiconductor portion has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline perovskite oxide layer.

231. The integrated circuit of claim 230, wherein the monocrystalline perovskite oxide layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline silicon substrate.

232. The integrated circuit of claim 223, wherein the integrated circuit has at least one feature selected from a group consisting of:

the monocrystalline perovskite oxide layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline silicon substrate; and

the monocrystalline perovskite oxide layer and the compound semiconductor portion have a lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.

233. An integrated circuit structure including:

a monocrystalline substrate layer having first and second regions;

a monocrystalline compound semiconductor layer overlying the second region of the monocrystalline substrate layer, the monocrystalline compound semiconductor layer being substantially lattice matched to the monocrystalline substrate layer through at least one crystallographically oriented, strain relieved, lattice compensated layer; and

an amorphous oxide layer located between the monocrystalline compound semiconductor layer and the monocrystalline substrate.

234. The integrated circuit structure of claim 233, further comprising a plurality of components located on or within one or more of the layers.

235. The integrated circuit of claim 234, wherein the components are electrical.

236. The integrated circuit of claim 234, wherein the components are optical.

237. The integrated circuit of claim 234, wherein the components are electrical and optical.--

REMARKS

By the above amendment original claims 1-143 have been canceled and new claims 144-193 have been added.

In view of the ample support for the newly presented claims Applicants submit that no new matter has been entered, and thus respectfully request examination on the merits.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Richard L. Treanor, Ph.D.
Attorney of Record
Registration No.: 36,379

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Claims 1-143 (Canceled)

Claims 144-237 (New)